

TITLE: A METHOD AND SYSTEM FOR IMPROVED ATE TIMING CALIBRATION AT A DEVICE UNDER TEST INVENTOR(S): Masashi Shimanouchi USSN: 10/773,698 Attorney Docket #: NPT-65.0403

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<u>100</u>

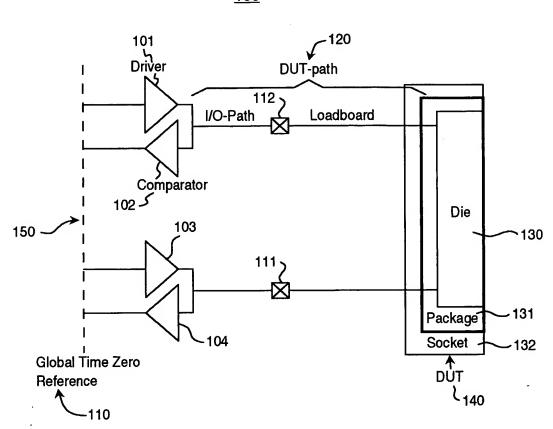


FIG. 1

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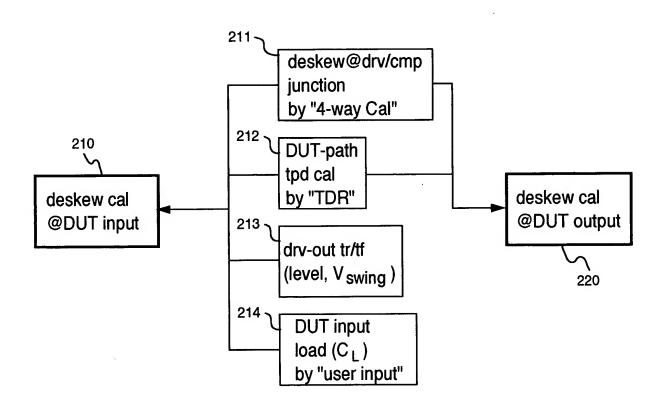


FIG. 2

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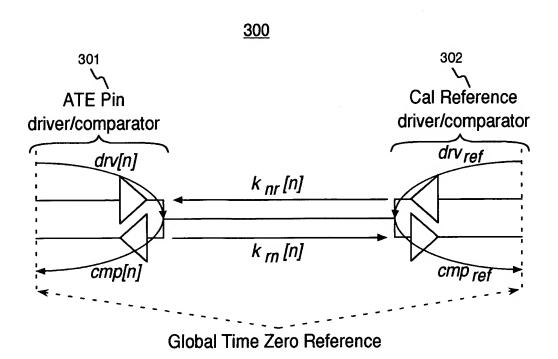


FIG. 3

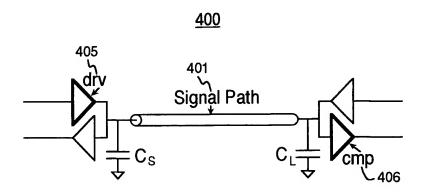


FIG. 4

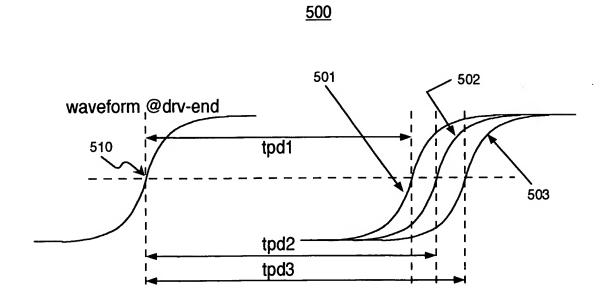


FIG. 5

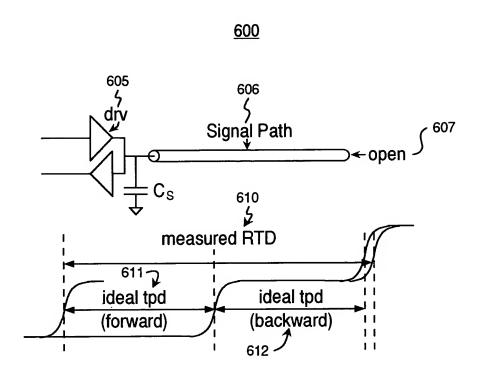
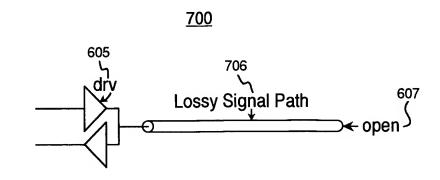


FIG. 6



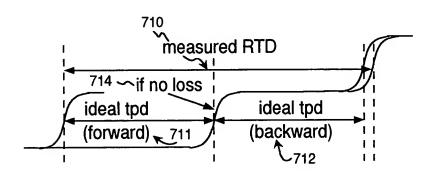


FIG. 7

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<u>800</u>

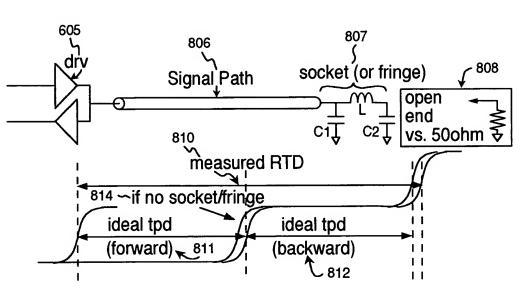


FIG. 8

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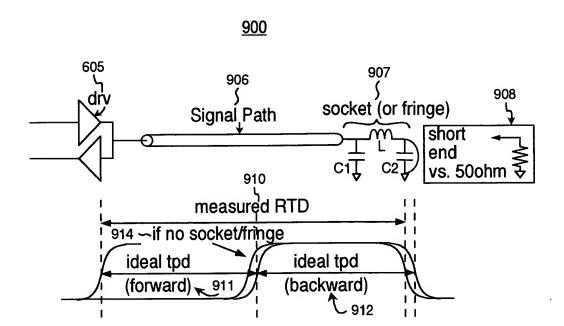


FIG. 9

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<u>1000</u>

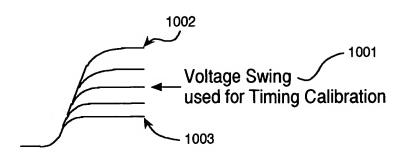
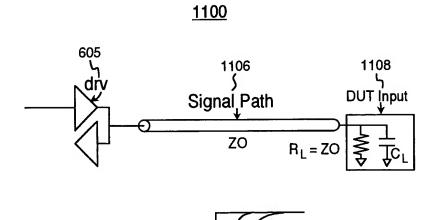


FIG. 10



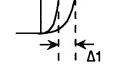


FIG. 11

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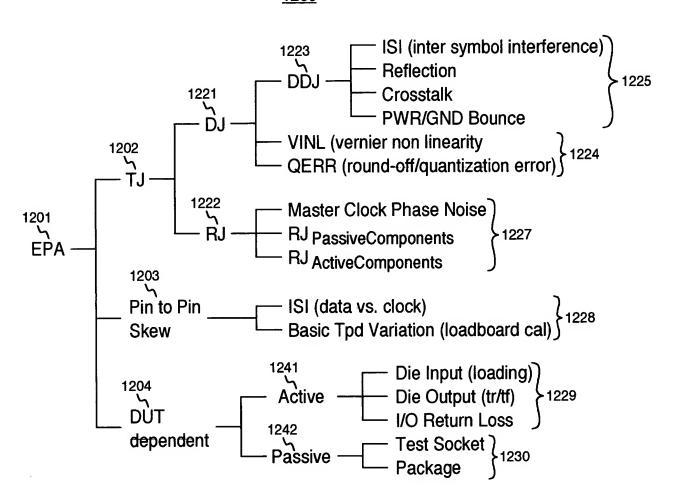


FIG. 12

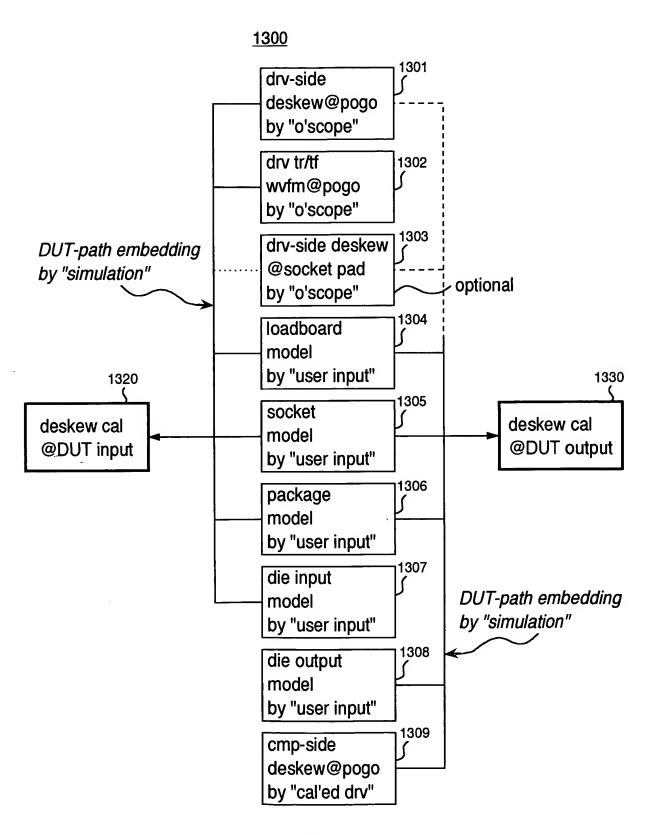


FIG. 13

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<u>1400</u>

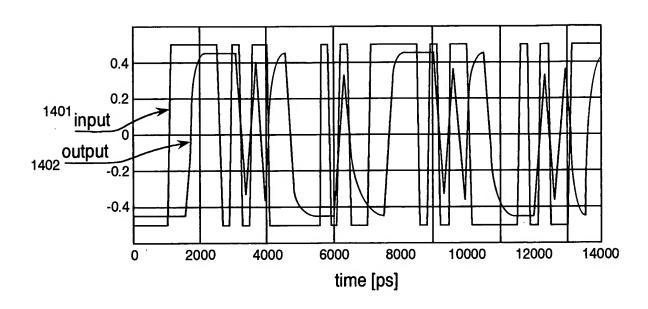


FIG. 14

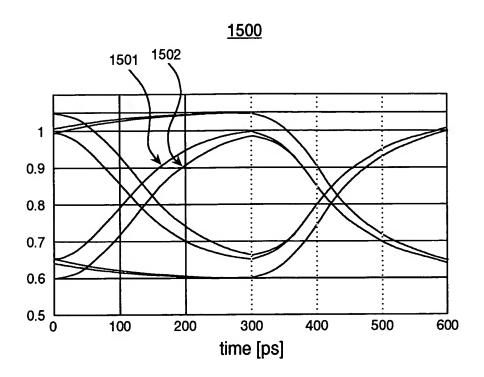


FIG. 15

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<u>1600</u>

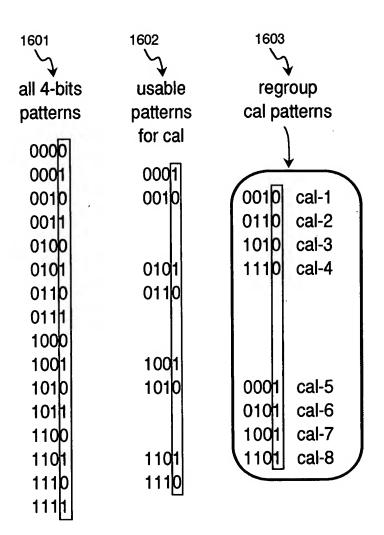


FIG. 16

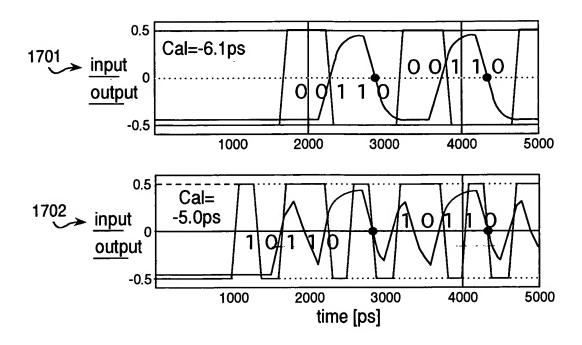


FIG. 17

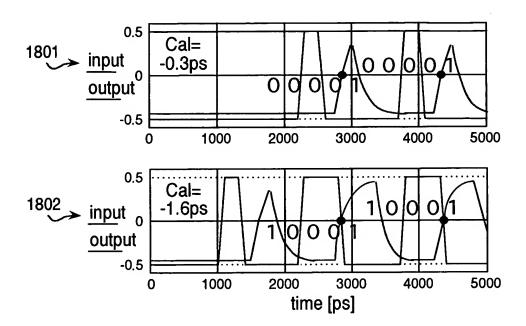


FIG. 18

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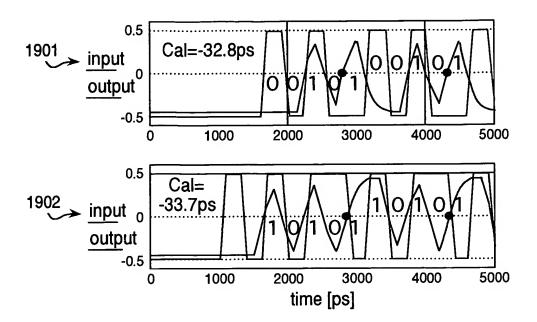


FIG. 19

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FIG. 20



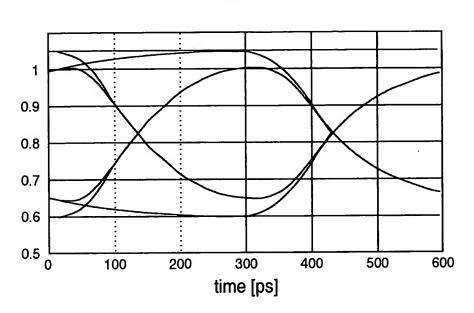


FIG. 21

TITLE: A METHOD AND SYSTEM FOR IMPROVED ATE TIMING CALIBRATION AT A DEVICE UNDER TEST INVENTOR(S): Masashi Shimanouchi

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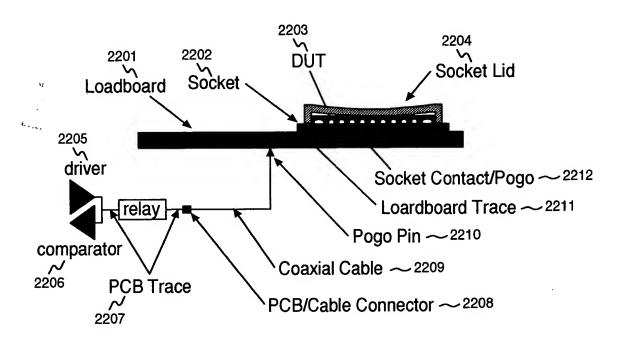


FIG. 22

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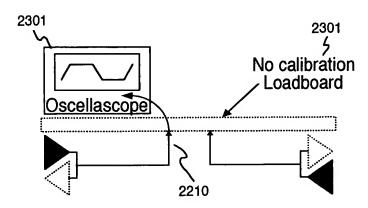


FIG. 23

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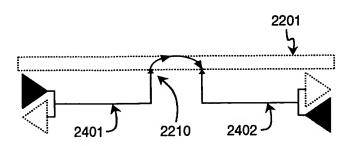


FIG. 24

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<u>2500</u>

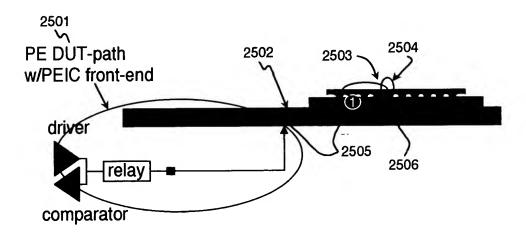


FIG. 25

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Device Load Board Device Load Board Socket DUT transistor level Fackage Die Tpd & DDJ

FIG. 26

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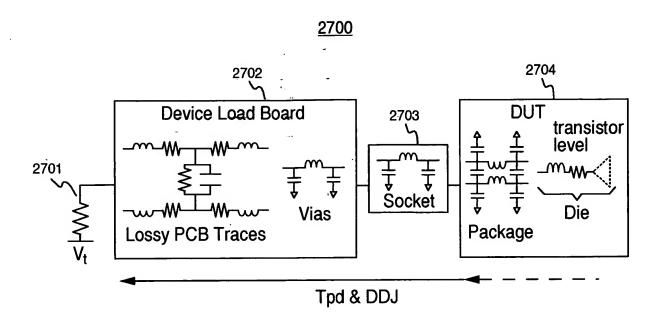


FIG. 27